REMARKS

The restriction requirement between article claims 1 to 11 and method-of-making claim 12 and applicants' election of claims 1 to 11 are acknowledged. The examined claims here are claims 1 to 11.

A new Abstract has been provided, which is believed to meet USPTO guidelines.

Various changes have been made in the specification, including that change on page 16 requested by the Examiner. The second full paragraph on page 18 has been revised to insert an element to number "11" for the shield layers shown in Figs. 3(A) and 3(B).

The independent claims have been amended better to point out that which applicants regard as their invention. The claims now state that each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs. Support for this change in the claims is found in the specification at page 15, lines 7 to 10, and page 17, lines 3 to 5.

The rejection of claims 1 and 9 under 35 USC 102 as anticipated by Sasao et al. '860, if applied to the claims as amended, is respectfully traversed.

It is agreed that Sasao et al. '860 describes a plasma display panel having various elements in common with the claimed invention and that the reference drawing at Fig. 1 shows phosphor layers 24R, 24G, and 24B. The pertinent description of that portion of Fig. 1

is found in the patent at column 3, lines 53 to 61. The reference, however, does not show a phosphor layer covering both the surface of the dielectric layer and the surface of the linear ribs within each pixel. Applicants have discovered that the arrangement as claimed calling for each of the phosphor layers (1) to extend intermittently in the lengthwise direction of the ribs for each pixel and (2) to cover the dielectric layer surface and the surface of the linear ribs within each pixel assures that the phosphor layers in the non-display region do not emit light even when ultraviolet rays generated through discharges in the display regions (pixels) in the plasma display panel. Accordingly, it is unlikely that the non-display regions are brightened, thus permitting the plasma display panel to display images that are both sharp and of high contrast. There is no such recognition or awareness in Sasao et al. '860. The rejection accordingly should be withdrawn.

The rejection of claims 1, 2, 9, and 10 under 35 USC 102 as anticipated by Ueoka et al. '345, if applied to the claims as amended, is also respectfully traversed. The reference discloses a plasma display panel again having many elements in common with the instantly claimed invention. The Examiner asserts that the reference at column 8, lines 44 to 45, describes linear ribs in that plasma display panel, that those ribs are located between the

address electrodes and phosphor layers are located between adjacent linear ribs so that there is intermittent extension in the lengthwise direction of the ribs for each pixel. Applicants respectfully disagree and submit that the drawings and the disclosure at column 8, lines 44 and 45, does not describe such linear ribs. Moreover, the phosphor layer shown in the drawings (see e.g. element 21d in Fig. 3) is not applied in the manner of the instant claims and the rejection should be withdrawn.

The rejection of claims 3 to 8 and 11 under 35 USC 103 as unpatentable over Sasao et al. '860 in view of Ueoka et al. '349 is also respectfully traversed. The references and their deficiencies have been discussed separately above. The references fail to teach or suggest the arrangement claimed herein, more particularly that each phosphor layer extends intermittently in the lengthwise direction of the ribs for each pixel and that the phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel. The rejection should be withdrawn.

Should any of the art rejections be maintained, the Examiner is asked to state on the record where either reference shows that the phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel.

The Examiner is thanked for acknowledging receipt of the certified copy of applicants' priority document and for listing the references provided with an Information Disclosure Statement. The Examiner is informed that a second Information Disclosure Statement accompanies this reply. He is asked to consider the references cited therein concurrently with the instant paper.

In view of the foregoing revisions and remarks, it is respectfully submitted that claims 1 to 11 are in condition for allowance, and a USPTO paper to those ends is earnestly solicited. The Examiner is requested to telephone the undersigned if additional changes are required in the case prior to allowance.

If the only barrier to allowance is the presence of non-elected method claim 12, he is authorized to cancel that claim for that express purpose.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

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a dielectric layer that covers the display electrodes, and a protective film as provided over the dielectric layer,

address electrodes formed on the back plate to run at right angles to the display electrode pairs, and a dielectric layer that covers the address electrodes, and

linear ribs provided between the address electrodes, with phosphor layers being so provided in each cell space formed by the adjacent linear ribs therebetween that they [are] not exist in the region on the back plate which corresponds to the region between the adjacent display electrode pairs for surface discharge on the front plate.

Preferably, the structure of the fifth aspect is further provided with shield layers as so formed in the region between the adjacent display electrode pairs for surface discharge on the front plate that they are parallel to the display electrode pairs.

Also preferably, this is still further provided with a dark layer on the entire surface below the linear ribs as provided between the address electrodes on the back plate and below the phosphor layers as provided in the cell spaces formed between the adjacent linear ribs.

The sixth aspect of the invention also to attain the object is a method for forming a phosphor screen of a plasma display panel, which comprises;

electrode pair X, Y for one pixel, it is desirable that the two are nearly the same. Taking the alignment error into consideration, it is desirable that the peripheral misregistration error falls within the range of ± 60 μm or so, preferably ± 30 μm or so, more preferably ± 10 μm or so. This is because if the surface area of the phosphor layers is too large, the first problem noted above could not be solved. On the other hand, if the surface area of the phosphor layers is too small, the plasma display panel will be dark.

10 In the PDP illustrated, the ribs 3 for partitioning discharge are present in the direction of the lines of the pairs of display electrodes X, Y for matrix display, but no ribs for partitioning discharge are present in the direction of the [liens] lines of the address electrodes 8 and the ribs 3. In the absence of such ribs, the distance between one pair of display electrodes and the neighboring pairs of display electrodes adjacent thereto shall fall between 200 and 600 μm. That distance therebetween is much larger than the discharge space (50 μm) between one display electrode X and the other display electrode Y to form one pair. In that situation, therefore, there occurs no abnormal discharge (discharge interference) between the 22 neighboring pairs of display electrodes adjacent to each other.

In the embodiment of the invention as illustrated in Fig. 2A and Fig. 2B, no phosphor layer is present in the spaces between the neighboring pairs of display electrodes adjacent to each

is baked to remove the organic component from the layers. According to that method, obtained is the back plate for PDP having the different color phosphor layers 10(R), 10(B) and 10(G) as patterned in an intended manner in predetermined cell spaces, as in Fig. 2B.

Fig. 3A and Fig. 3B are structural views showing another embodiment of the plasma display panel of an AC mode of the invention. Precisely, Fig. 3A is a cross-sectional view of Fig. 3B as cut along the line B-B that runs through one address electrode vertically thereto; and Fig. 3B is a view showing the pattern of phosphor layers as provided in cell spaces between adjacent ribs.

In the plasma display panel of Fig. 3A and Fig. 3B, shield layers are formed between the adjacent display electrode pairs, running in parallel to the display electrodes. In this, the phosphor in the display regions emits light, while the display regions are shielded from light that leaks from the non-display regions. Therefore, the PDP could produce sharp images.

In the embodiments of Figs. 2A and 2B and Figs. 3A and 3B, it is more desirable that the dielectric layer 9 which covers the address electrodes on the back plate acts as a light-absorbing layer. For this, the dielectric layer 9 may be a dark layer acting as a light-absorbing layer. Though not shown, an additional dark layer may be provided over the dielectric layer 9 to attain the same effect. However, using the dielectric

MARK-UP

(Amended)

1. A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located between the adjacent linear ribs so that they each extend intermittently in the lengthwise direction of the ribs for each pixel.

, wherein each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel

(Amended)

3. A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a light-absorbing layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located between the adjacent linear ribs so that they each extend intermittently in the lengthwise direction of the ribs for each pixel.

wherein each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel

5. (Amended) A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a transparent sustain electrode and a non-transparent metal bus electrode,

a translucent dielectric layer covering the display electrodes, and a magnesium oxide-containing, translucent protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dark dielectric layer covering the address electrodes,

linear ribs located between the address electrodes, and phosphor layers as so provided between the adjacent linear ribs so that a red-emitting phosphor layer, a blue-emitting phosphor layer and a green-emitting phosphor layer adjacent each other with a rib therebetween and these three different phosphor layers each extend intermittently in the lengthwise direction of the ribs.

, wherein each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs

(Amended)

7. A back plate for plasma display panels, which comprises;

a plurality of linear address electrodes on a glass substrate, a dark dielectric layer covering the address electrodes, and linear ribs between the address electrodes, and

phosphor layers located between the adjacent linear ribs so that a red-emitting phosphor layer, a blue-emitting phosphor layer and a green-emitting phosphor layer are adjacent each other with a rib therebetween and these three different phosphor layers each extend intermittently in the lengthwise direction of the ribs,

wherein each phosphor layer covers both the surface of the dark dielectric layer and the surface of the ribs

(Amended)

9. A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with a phosphor layer located in each of a plurality of adjacent cell spaces formed by a plurality of adjacent linear ribs, said phosphor layers being intermittently interrupted so that they do not exist in the regions on the back plate which correspond to the region between the adjacent display electrode pairs.

wherein each phosphor layer covers the surface of the dielectric layer and the surface of the linear ribs